

ABSTRACT

5 The present invention includes a memory subsystem comprising  
at least two semiconductor devices, including at least one memory  
device, connected to a bus, where the bus includes a plurality of  
bus lines for carrying substantially all address, data and  
control information needed by said memory devices, where the  
control information includes device-select information and the  
bus has substantially fewer bus lines than the number of bits in  
a single address, and the bus carries device-select information  
without the need for separate device-select lines connected  
directly to individual devices.

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20 The present invention also includes a protocol for master  
and slave devices to communicate on the bus and for registers in  
each device to differentiate each device and allow bus requests  
to be directed to a single or to all devices. The present  
invention includes modifications to prior-art devices to allow  
them to implement the new features of this invention. In a  
preferred implementation, 8 bus data lines and an AddressValid  
bus line carry address, data and control information for memory  
addresses up to 40 bits wide.